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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/469,409	12/22/1999	BRIAN A. PETERSEN	M-7907-US	4940

33031 7590 08/19/2002

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EXAMINER
POLLACK, MELVIN H

ART UNIT	PAPER NUMBER
2152	3

DATE MAILED: 08/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/469,409	PETERSEN ET AL.	
	Examiner	Art Unit	
	Melvin H Pollack	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 1999* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *see attached office action* .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-3, 6, 7, 13-17, 20-22, and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Muller et al. (6,128,666).

6. For claim 1, Muller teaches a method (see abstract) of packet processing (col. 1, lines 10-15) comprising:

a. Parsing a packet, said packet having a header portion, to determine a vector (col. 6, lines 5-10);

b. Coordinating processing using said vector (col. 6, lines 18-25);

c. Deconstructing said packet header to form header data (col. 6, lines 5-10, where it is anticipated that the extraction of header data from the header is a required first step to analysis of the aforementioned header data.);

d. Searching one or more data structures based on said header data to produce search results (col. 6, lines 26-32);

e. Editing said packet based on said search results, said header data, and said vector (col. 6, line 66 – col. 7, line 3);

f. Said coordinating further comprises monitoring said deconstructing, said searching, and said editing (col. 3, lines 62-65).

7. As for claim 2, Muller teaches that said coordinating further comprises sharing data with said parsing, said deconstructing, said searching, and said editing (Fig. 3).

8. As for claim 3, Muller teaches that said packet is buffered before said parsing (col. 6, lines 1-2).

9. For claim 6, Muller teaches an apparatus (see abstract) for packet processing, comprising:

a. A central processor for packet processing, said central processor comprising a register set (col. 3, lines 55-62); and

b. One or more peripheral processors each connected to said central processor and each comprising a register set (col. 3, lines 56-58), wherein each said peripheral processor returns at least one datum to said central processor (Fig. 2); wherein

c. Said central processor communicates with said peripheral processor (col. 3, lines 62-65).

10. As for claim 7, Muller teaches that the central processor comprises a general purpose processor (col. 3, line 59, and col. 10, lines 28-32. It is anticipated that the processor can participate in a variety of functions, making it a general purpose processor.).

11. As for claim 13, Muller teaches that a portion of each said peripheral register set is mapped onto said central processor register set (col. 3, lines 60-62).

12. As for claim 14, Muller teaches that said central processor and at least one peripheral processor together form at least a part of a single application specific integrated circuit (col. 4, lines 20-34).

13. Claims 15-17 are drawn to a computer system for packet processing, comprising computer instructions for implementing the method drawn in claims 1-3, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 1-3 are rejected, then claims 15-17 are also rejected for the reasons above.

14. Claims 20-22 are drawn to a computer-readable storage medium, comprising computer instructions for implementing the method drawn in claims 1-3, respectively. It is considered in

the prior art that a system implementation is logically equivalent to the underlying method. Official notice is also taken that computer instructions would be stored on a computer-readable medium such as a disk or memory. Therefore, if claims 1-3 are rejected, then claims 20-22 are also rejected for the reasons above.

15. Claims 25-27 are drawn to a computer data signal embodied in a carrier wave, comprising computer instructions for implementing the method drawn in claims 1-3, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 1-3 are rejected, then claims 25-27 are also rejected for the reasons above.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1-7, 13-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claims 1-3, 6, 7, 13-17, 20-22, and 25-27 above, and further in view of Turner et al. (6,018,524).

18. For claims 1-3, 6, 7, 13-17, 20-22, and 25-27, that which is anticipated is obvious.

19. As for claim 4, Muller does not go into detail regarding the nature of the search method, treating it as a black box. Turner, which goes into significant detail regarding search methods in the process of packet analysis and routing, teaches that said deconstructing further comprises forming a search argument, and said searching uses said search argument (col. 7, lines 25-34). Further, this step would be obvious under Muller, due to the claim 1 discussion above, since the extraction of data for search purposes would automatically make said data a "search argument" by definition. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use Turner's router search method in Muller's router search black box as a way of implementing that particular feature.

20. Claim 5 has many of the same limitations as claim 4. However, the method further consists of said coordinating further comprises operating on said search argument to form a modified search argument prior to said searching, and said searching uses said modified search argument. Turner also teaches the modification of a search argument (col. 11, lines 15-18). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use Turner's router search method in Muller's router search black box as a way of implementing that particular feature.

21. Claims 18 and 19 are drawn to a computer system for packet processing, comprising computer instructions for implementing the method drawn in claims 4 and 5, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 4 and 5 are rejected, then claims 18 and 19 are also rejected for the reasons above.

22. Claims 23 and 24 are drawn to a computer-readable storage medium, comprising computer instructions for implementing the method drawn in claims 4 and 5, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Official notice is also taken that computer instructions would be stored on a computer-readable medium such as a disk or memory. Therefore, if claims 4 and 5 are rejected, then claims 23 and 24 are also rejected for the reasons above.

23. Claims 28 and 29 are drawn to a computer data signal embodied in a carrier wave, comprising computer instructions for implementing the method drawn in claims 4 and 5, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 4 and 5 are rejected, then claims 28 and 29 are also rejected for the reasons above.

24. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claim 6 above, and further in view of VanDervort et al. (5,761,191).

25. For claim 8, VanDervort teaches that the central processor comprises a microsequencer (col. 7, lines 7-9). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a microsequencer CPU in Muller's invention to fulfill the necessary implementation aspects.

26. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claim 6 above, and further in view of Vahalia et al. (6,275,953).

27. For claim 9, Vahalia teaches that the central processor comprises more than one processor acting in concert (col. 2, lines 6-9). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a parallel processor CPU in Muller's invention to fulfill the necessary implementation aspects and to make the invention more flexible and less prone to error.

28. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claim 6 above, and further in view of Eames et al. (6,078,593).

29. For claim 10, Eames teaches that one or more of said peripheral processors comprise fixed logic circuits (col. 21, lines 1-5). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a fixed logic peripheral processor in Muller's invention to fulfill the necessary implementation aspects.

30. As for claim 11, Eames teaches that one or more of said peripheral processors comprise programmable logic circuits (col. 21, lines 1-5). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of

ordinary skill in the art would have used a programmable logic peripheral processor in Muller's invention to fulfill the necessary implementation aspects.

31. As for claim 12, Eames teaches that one or more of said peripheral processors comprise a programmable state machine (col. 21, lines 44-48). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a programmable state machine peripheral processor in Muller's invention to fulfill the necessary implementation aspects.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Civanlar et al. (5,996,021) teaches a method of routing from ingress to egress router. Hauser et al. (6,426,957) and Smith (6,188,686) teach ATM switch background information. Eriksson et al. (6,423,384) teaches an implementation of an ATM switching table. Bonomi et al. (6,219,352) teaches ATM cell switching background and cell/packet queues. Johnson et al. (6,301,257) teaches the study of a packet header in network switching. And Oguchi et al. (6,304,912) teaches background information on the learning processes of a switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin H Pollack whose telephone number is (703) 305-4641. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on (703) 308-4815. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MHP
August 14, 2002

ROBERT B. HARRELL
PRIMARY EXAMINER